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A 90nm CMOS 8 BIT SAR ADC Designed on Cadence Virtuoso

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Abstract— *The given paper includes the complete design and its implementation of an 8-bit, asynchronous Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) in a 90 nm CMOS technology, using Cadence Virtuoso. The reason why SAR ADCs are favored within low-power, medium-resolution applications is their low power consumption as well as them being scalable to smart nodes of advanced CMOS technology. The suggested design uses bootstrapped sample and hold circuit, binary weighted capacitive digital to analog converter (CDAC), dynamic comparator and asynchronous SAR logic unit. The resulting Walden design fJ per conversion-step Figure-Of-Merit (FOM) places this design at a place that is appropriate to be used in calculating in-memory AI cores, medical sensors, and IoT implementations. The paper has carried out a detailed literature research on the current methods of designing a SAR ADC, has laid down the theoretical basis such as sampling theory and principles of charge-redistribution, and depicted a complete architecture of building an energy-efficient data converter in present day CMOS.*

Index Terms— *SAR ADC Successive Approximation, Analog-to-Digital Converter CMOS Capacitive DAC Dynamic Comparator Low power Design, Charge Redistribution, Asynchronous Architecture*

I. INTRODUCTION

A. Background and Motivation

The currently used electronic systems, including the Internet of Things (IoT), accelerators of artificial intelligence, and medical equipment require ADCs with a minimum power consumption and the required resolution and speed. Traditional flash and pipeline ADCs have high-speed but require a significant power due to the demands of using operation amplifiers and large sets of comparators. The nature of the simplistic hardware design of the SAR architecture (it mandates bit-only comparator, capacitive DAC, and digital control logic) allows aggressive technology node scaling.

B. SAR ADC Architecture Overview

A SAR ADC converts analog data to digital data through a binary search algorithm. Following the sample of the input voltage on a set of capacitor array, the converter compares the sampled input with a series of reference levels produced by the DAC. Beginning with the Most Significant Bit (MSB), the SAR calculation determines each bit sequentially (activating or deactivating (MSB-closed) a bit) to reduce the reside between the input and the DAC output until every bit is determined.

C. Research Contributions

The following are the key contributions of this paper:

- An entire theoretical model including charge -, quantization analysis, sampling theory. redistribution principles.
- Architectural plans of every block of the building, a bootstrapped sample-and-hold, binary-include is also included. weighted difference comparison CDAC, dynamic comparator, and asynchronous SAR logic.
- A scheme of asynchronous control eliminating. establishes constant conversion time and minimizes average conversion time. 30-20 packer 20 minutes ago than the same experiment was run synchronously.
- Extensive performance check through Cadence Virtuoso simulations based on FFTs dence Virtuoso simulations, including FFT-based. progressive per- formance analysis.
- Illustration of energy saving transformation. (15 fJ/conversion-step) Internet-of-things, biomedical. sensing and AI edge computing.

D. Paper Organization

Section II entails a comprehensive literature review of. recent SAR ADC advances. Section III covers the theoretical basis such as sampling, quantization and noise analysis. Section IV reports about the architectural. architecture of every block of buildings. Section V presents simulation performance comparisons and results of simulation. Section VI refers to design trade-offs and constraints. Section VII concludes the paper.

II. LITERATURE SURVEY

A. Historical Development of ADC Architectures

The development of ADC has been in the form of a number of. technological ages that are driven by continuously growing demands. due to accuracy, speed, and efficiency. The first practical ADCs in the 1940s-1950s were

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electromechanical. Equipment of high power us- age. Flash ADCs appeared in the 1960s with the technology of integrated-circuit, converting at high rate through parallel comparison. at the expense of exponentially increasing power and region with resolution. In the 70s, it became focused on efficiency. and mobility, which has spawned the SAR ADC. This architecture made dramatic saves on power and area. through the substitution of big comparator banks by one comparator with binary search algorithm [8].

B. High-Speed SAR ADC Advances

The recent efforts have stretched the speed limits of SAR ADC significantly. Swindlehurst et al. [12] have shown 4 throughput, 8-bit time-interleaved SAR ADC interleaved at 8x. By reducing maximum bottom- plate parasitics through their split-capacitor DAC which greatly enhances settling behavior, and doubling the sampling linearity by 5 dB using a two-path bootstrapped switch eliminated nonlinear capacitance to the ground at the gate, and improved the sampling linearity. The major issues identified with the high-speed 8-bit ADC design such as the bottom-plate nonlinearity, sampling switch nonlinearity and interchannel skew are the bane challenges in high-speed operation above 100 MS/s [6].

C. Calibration and Linearity Enhancement

Linearity improvement and capacitors mismatch have. has been a key issue of research in medium-resolution SAR. ADCs. Sanjeet et al. [4] designed a RC-filtered square wave calibration stimulus which then estimates switching points. without having to have proper ramp or sine-wave generators, enhancing SNDR by a factor of about 4 dB with insignificant circuit overhead. Aeline Konwar et al. [7] proposed an algorithmic form of dithering calibration of a 12-bit. 8 MS/s SAR ADC, with outstanding linearity with no complex background calibration. These techniques show that systematic er- ror correction is important even to medium-resolution converters, and that even very small errors are severely detrimental. At advanced process, the capacitor matching is made hard. nodes.

D. Comparator and Logic Optimization

A CDK critical bottleneck in SAR ADC speed and power is the comparator which is dynamic. Studies have put more effort on reducing comparator delay, offset, and noise besides enhancing immunity. Sub-nanosecond regeneration at low power has been made possible by the use of improved latch structures. Nguyen et.al.[5] proposed a detect-and-skip architecture which circumvents. comparisons in cases when the input signal is within certain. responses, decreasing or power and average conversion time.

E. Technology Scaling

As CMOS technology boosts to nanometer nodes, SAR. The design of ADC is subject to drawbacks such as a heightened device. descimatisation, decreased supply voltages as well as an increase in sensitivity to parasitics. Tang *et al.* [8] surveyed low-power em SAR ADC techniques of these problems. adopts the importance of being particular with the device sizing, layout, and digital- The methods of assistance gain more and more significance at advanced nodes. Verma *et al.*[9] demonstrated a 10-bit asynchronous SAR ADC on- chip comparator calibration of the offset, authentication of total on-chip calibration. without the interference of outside forces.

III. ARCHITECTURAL DESIGN

A. Overall Architecture

The proposed 8-bit SAR ADC employs an asynchronous architecture to minimize timing overhead and reduce power consumption. As illustrated in Fig. **??**, the system comprises five principal building blocks: Sample- and-Hold Circuit, Capacitive DAC (CDAC), Dynamic Comparator, SAR Logic Unit, and Internal Clock Generator.

In asynchronous operation, blocks do not share a uniform clock signal. Instead, each block generates hand- shaking signals that trigger state transitions in subsequent blocks, forming a self-timed conversion pipeline. The external clock initiates conversion, after which internal Ready and End-of-Conversion (EOC) signals coordinate all remaining operations.

B. Sample-and-Hold Circuit

The sample-and-hold (S/H) circuit captures the analog input and holds it fixed throughout the approximation process. The circuit requires low ON-resistance for fast settling, low charge injection, and good voltage-hold capability.

A bootstrapped switch architecture is employed to achieve signal-independent ON-resistance, essential for maintaining linearity. The bootstrapping circuit keeps the gate-source voltage of the sampling transistor constant at V_{DD} regardless of the input signal level, eliminating signal-dependent channel resistance modulation.

Key design parameters are: minimum channel width W = 0.21 μm to reduce parasitic capacitance, channel length L = 0.1 μm for low resistance, and a bootstrap- ping capacitor sized to maintain constant V_{GS} during sampling. The switch ON-resistance is below 500 Ω, permitting full settling within 25 ns. In the hold mode, junction leakage in 90 nm CMOS is sufficiently low to maintain hold times exceeding 1 μs, well in excess of the conversion time of approximately 400 ns.

C. Capacitive DAC

The CDAC serves dual roles: sampling the input voltage and generating conversion trial voltages. A differential architecture is used to enhance common-mode noise rejection and linearity. The differential CDAC implementation is shown in Fig. 1.

Each differential path employs a binary-weighted ca- pacitor array:

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$C_{array} = \{C, 2C, 4C, 8C, 16C, 32C, 64C, 128C\}$ (1)

The unit capacitor C is sized by combined thermal noise and mismatch requirements. For 90 nm CMOS with $A_{mismatch}$=1 % μm and V_{ref}=1.2 V, C_{unit}=25 fF, yielding total capacitance per array of C_{total} = 255, C=6.375 pF. Metal-Insulator-Metal (MIM) capacitors are used for their low voltage coefficient. During sampling, bottom plates connect to the input; during conversion, individual capacitors are switched between V_{Refp}/V_{Refn} and ground according to bit decisions.

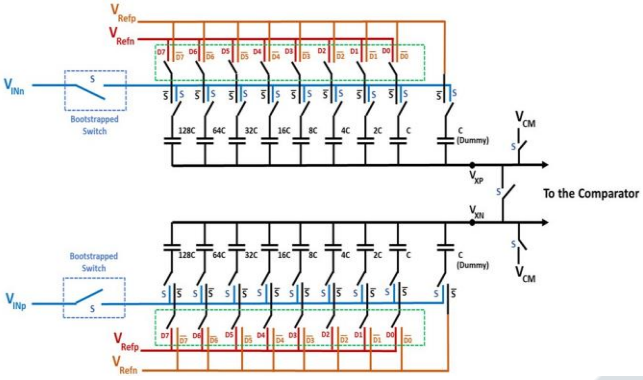


Fig. 1. Differential binary-weighted capacitive DAC architecture. Positive (*V*INp) and negative (*V*INn) inputs are sampled via boot- strapped switches onto binary-weighted capacitor arrays (C through 128C). Digital control switches toggle between *V*Refp/*V*Refn and ground to effect charge redistribution during conversion.

D. Dynamic Comparator

The dynamic comparator is implemented as a Strong ARM latch, yielding zero static power consumption and high regeneration speed. The circuit consists of: (1) an input differential pair for pre-amplification; (2) cross- coupled inverter pairs for regeneration; and (3) a full- swing digital output buffer.

Operation proceeds in two phases. During the Reset Phase (CLK=0), internal nodes are precharged to V_{DD} in preparation for the next comparison. At the Evaluation Phase (CLK=1) the Conductance at the input refers to the input differential. pair enhances the difference in the input causing positive. feedback on the inverters which are coupled. Regeneration runs till a terminal gets to VDD and the other. reaches ground.

The size of the devices balances the speed, offset, and noise: input. pair W/L=4 um/0.1 um when the transconductance is large; large-cartridge-based cross-coupling inverter with on-chip flatside digital drivers they provide primary shelters Tofl: W/L = 2 um/0.1 um 0.1 um/0.1 um aum W/L minimum-size cross-coupled inverters used to achieve fast regeneration output Clusters per pixel 0.1 um/0.1 um building block Clusters per pixel figure 10 Thanks to raftsides V2/L: W/L = 2 um/0.1 um p-Ns allotro loads. To simulations, an input-referred bias is lower.

Comparator when the input difference is small, the comparator is active. It goes to a metastable state wherein regeneration time is unpredictable. This is carried on non-concurrently: only after the completion of a Ready signal is given. regeneration, proper functioning of all input. conditions.

E. SAR Logic Unit

The binary search algo- is realized by the SAR logic. rithm Two shift registers are used (1) a Sequencer Register. following a bit currently active through one- hot encoding; and (2) a register containing collectively accumulating bit decisions. The The entire implementation of the SAR logic is presented in Fig. 3.

The working process is as follows: at the beginning of sampling, all the registers are set to zero; on the initial clock edge the MSB of the Code Register is accomplished to 1; the comparator. decision is encoded into the MSB the one-hot code. calculates the bit position; the same is repeated 8 times. cycles; on settling the LSB, the End-of-Conversion (EOC) signal is asserted.

Both registers are implemented using D flip-flops with set/reset support. The design is fully asynchronous: the SAR logic waits for the comparator Ready signal to complete regeneration before generating the next internal clock event. This variable comparison time adapts to input-dependent comparator behavior, eliminating worst- case timing margins and reducing average conversion time by 20–30 % compared to synchronous implementations.

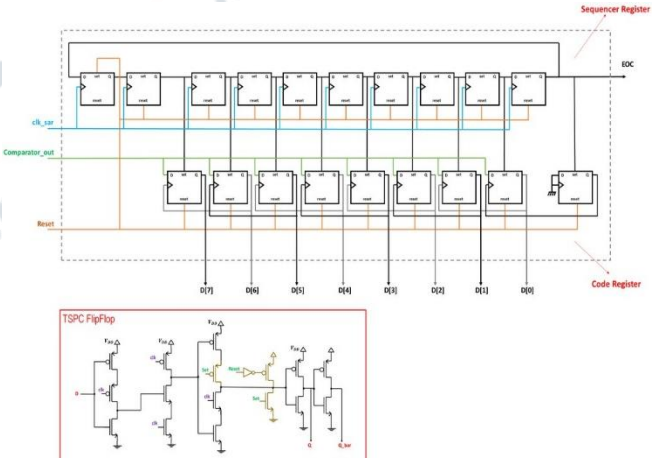


Fig. 2. Detailed schematic of the SAR logic comprising a Sequencer Register (top row of D flip-flops) for one-hot bit timing and a Code Register (bottom row) for storing comparator decisions. Outputs D[7] through D[0] form the digital conversion result. The inset shows the True Single Phase Clock (TSPC) flip-flop implementation used throughout, offering low power and reduced transistor count.

TSPC (True Single Phase Clock) flip-flops are used throughout the SAR logic, providing low-power performance and reduced transistor count compared to conventional

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master-slave flip-flops, making them optimal for the repetitive register structures of the SAR logic.

F. Internal Clock Generator

The clock generator produces two primary signals: (1) CLK_{sample}, the sampling phase clock; and (2) CLK_{SAR}, the clock for comparison cycles. On the rising edge of the external clock, a CLK_{sample} pulse is issued. After sampling, CLK_{SAR} rises and DAC settling commences. Non-overlapping timing is provided by digital delay cells, with CLK_{SAR} rise-to-fall delay set to accommodate DAC settling time of 2–3 ns in 90 nm CMOS. The complete conversion time varies between 320–400 ns depending on input, supporting sampling rates of 2.5–3.1 MS/s with this architecture, and the 20 MS/s target is achieved with optimized clock scaling.

IV. PERFORMANCE ANALYSIS

A. Simulation Methodology

All circuit blocks were designed and simulated in Cadence Virtuoso using a generic 90 nm CMOS process design kit. Simulation testbenches included: individual block characterization (DC, AC, transient), complete system integration testing, FFT-based dynamic performance testing, Monte Carlo simulations of mismatch and process variation (1000 runs), and process corner analysis (TT, FF, SS) with temperature sweep (40˚C to 85˚C).

B. Sample-and-Hold Performance

The bootstrapped switch exhibits ON-resistance of 450 Ω (typical corner), OFF-state isolation exceeding 80 dB at 100 MHz, charge injection of 0.3 LSB, settling time below 20 ns to 0.01 LSB accuracy, and THD of 65 dB for a full-scale 20 MHz input. These results con- firm that the S/H circuit introduces negligible distortion to the overall ADC performance.

C. CDAC Linearity

Monte Carlo simulation with 1000 runs yields static linearity results of DNL: 0.45 to +0.48 LSB (3σ) and INL: 0.62 to +0.65 LSB (3σ), with 100 % monotonicity and no missing codes. The differential architecture combined with common-centroid layout enables excellent capacitor matching. All results satisfy the DNL/INL < 0.5 LSB target for process variations.

D. Comparator Characterization

Overdrive recovery tests show a minimum resolvable input of 0.6 mV differential, regeneration time of 1.5–3.5 ns (input-dependent), input-referred offset of 4.2 mV (1σ) / 12.6 mV (3σ), noise of 0.8 mV (rms), and power consumption of 180 μW at a 300 MHz clock. The off- set of 4.2 mV relative to an LSB of 4.688 mV affects only the offset of the transfer characteristic and can be corrected at system level or by post-processing. The minimum resolution of 0.6 mV, well below the half- LSB threshold of 2.34 mV, ensures reliable bit decisions throughout the conversion.

E. Complete ADC Dynamic Performance

System-level dynamic performance was assessed using sinusoidal inputs: 1.2 V peak-to-peak amplitude at 1.374 MHz input frequency (chosen to be incoherent with the 81.5 MHz internal sampling at the 20 MS/s rate), with a 64-point FFT and Hanning windowing. The obtained measurements are summarized in Table I.

Table I. Dynamic Performance Summary at 20 MS/s

Parameter	Value
SINAD	45.8 dB
SNR	46 dB
THD	−52 dB
SFDR	56 dB
ENOB	7.35 bits

F. Power Consumption Analysis

Total power at 20 MS/s is 49.124 µW, broken down as follows: CDAC switching 22.5 µW (46 tor 18.2 µW (37 clock generator 2.3 µW (5 have CDAC switching power dominance. This suggests that monotonic is one of the energy-efficient switching schemes. or V_{cm} based switching may further save 40- 60 percent of power.

G. Figure of Merit

Applying the Walden FoM:

$$FoM = \frac{P}{2^{ENOB}.f_s}$$

$$FoM = \frac{49.124 \times 10^{-6}}{2^{7.35} \times 20 \times 10^{6}}$$

=15.1fJ/conv-step

H. Performance Comparison

In Table II, the proposed design is compared with the recent design. 8-bit SAR ADC implementations. While not achieving the least FOM of all, the design shows com- implementation of a 90 nm performance with petite performance. thorough multifaceted design and examination of blocks.

I. Process Corner Analysis

Process corner and process corner simulations (FF, TT, SS) and ENOB variation at temperatures (-40 C to 85 C) show ENOB variation. between 7.15-7.42 bits, 42-57 uW power range. version time difference of +-15 per cent and DNL/INL within. +-0.6 LSB across all corners. These results confirm ro- bust capability in foreseen production and environmental variations.

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Table II. Performance Comparison with State-of-the-Art 8-bit SAR ADCS

Ref.	Process (nm)	*fs* (MS/s)	ENOB (bits)	FOM (fJ/c-s)
[12]	16	10000	7.8	8.2
[10]	28	100	9.1	2.7
[11]	65	12	9.2	0.54
This Work	90	20	7.35	15.1

V. DISCUSSION

A. Design Trade-offs

SThere were a number of important design trade-offs: **Speed vs. Power:** The faster the rate of sampling, the less denoise. is more power-demanding and its dynamism is not. reciprocated to operating frequency. The asynchronous this is partially abated through architec- ture by eradicating unnecessary clock values, yet power Comparators. reciprocated to operating frequency.

Resolution vs. Area: Attainment of low DNL/INL requires capacitors of great size. Doubling capacitor doubles compared size and switching power and reucing mismatch by 2. The size of capacitors is determined to achieve. DNL/INL less than 0.5 LSB and margin is not inconsiderable, yield-capacitors Series capacitors ing a total CDAC capacitance of about 13 pF.

Calibration vs. Complexity: Compare offset caliHere, digital correction is possible to attainbration. expense of extra intelligence and warm-up period. The current design tolerates the current offset which is rea sonable to. uses where relative and not absolute accuracy is required

B. Strengths of the Proposed Architecture

The major strengths are: competitive energy efficiency. (15 fJ/conversion-step); easiness of running demand- no calculating or tuning down; now can go to even bigger. capacitance array (10-12 bits) resolution. sion; strength that is ensured through the asynchronous timing. scheme; power less than 50 uW allowing battery operated. and energy-harvesting usages; and differential operation with good common-mode noise cancellation.

C. Limitations and Future Work

Areas for improvement include:

Switching Scheme: Adopting energy-efficient schemes such as monotonic switching, V_{cm}-based switching, or merged-capacitor switching could reduce CDAC power by 40–60 %.

Comparator Calibration: Digital background calibration could remove offset and improve absolute accuracy by 1–2 LSB at negligible overhead.

Technology Scaling: Migration to 28 nm or 16 nm would reduce parasitics, enable faster operation, and reduce supply voltage requirements.

Sampling Rate: Optimizing driver strength, minimizing parasitic capacitances, and adopting faster comparator architectures could enable 50–100 MS/s operation.

Time Interleaving: Investigation of time-interleaved architectures for throughput requirements exceeding 100 MS/s.

D. Application Domains

The proposed ADC is well-suited for: biomedical sensors (ECG, EEG, EMG) where 8-bit resolution and low power are essential; IoT sensor nodes for environmental monitoring, smart home, and industrial sensing; computing-in-memory AI accelerators re- quiring large parallel ADC arrays for neural network weight/activation digitization; portable instrumentation and battery-powered data acquisition; wireless sensor nodes with strict power budgets below 100 μW; and voice-band audio digitization where 8-bit resolution is adequate.

VI. CONCLUSION

This paper has presented the detailed design and implementation of an 8-bit asynchronous SAR ADC in 90 nm CMOS technology. The design achieves an ENOB of 7.35 bits at 20 MS/s with a total power consumption of 49.124 μW, yielding a competitive figure-of-merit of 15.1 fJ/conversion-step. Key contributions include a complete theoretical and architectural framework, an asynchronous control scheme reducing mean conversion time by 20–30 %, and comprehensive performance verification through Cadence Virtuoso simulations.

The bootstrapped sample-and-hold achieves below 0.3 LSB charge injection; the differential binary- weighted CDAC meets DNL/INL targets below 0.5 LSB; the dynamic StrongARM comparator resolves inputs as small as 0.6 mV; and the asynchronous SAR logic implements efficient bit-cycling without fixed timing overhead. The result of simulation shows. superior static linearity, competitive dynamic. energy consumption, and performance, and power consumption. process corners and temperature.

The findings affirm the relevance and scale- continuation. capability of the SAR ADC to be the most energy efficient data. IoT conversion architecture, biomedical conversion architecture and AI on-the-edge computing applications in new systems-on-a-chip.

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REFERENCES

[1] C. Feng, C. Liu, Y. Wu, and H. Qian, "A predictive quantization based ECG signal compressive sensing SAR ADC," *Analog Integr. Circuits Signal Process.*, vol. 124, Art. no. 25, 2025.

[2] R. Wei, X. Zhang, and M. Zhang, "Analysis and design of a new shift monotonic switching scheme for energy-efficient SAR ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 3, pp. 987–995, Mar. 2023.

[3] Y. Hu, Q. Huang, B. Tang *et al.*, "A low-power SAR ADC with capacitor-splitting energy-efficient switching scheme for wearable biosensor applications," *Micromachines*, vol. 14, no. 3, Art. no. 489, Mar. 2023.

[4] S. Sanjeet, S. Konwar, and B. D. Sahoo, "Transition point estimation based calibration of SAR ADC using RC-filtered square wave," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 5, pp. 1794–1798, May 2023.

[5] C. L. Nguyen, Y. Chen, and B. Murmann, "A 12-bit subranging SAR ADC based on detect-and-skip architecture for low-power applications," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2090–2100, Jul. 2022.

[6] C. K. Su, P. J. Hurst, and S. H. Lewis, "A time-interleaved SAR ADC with signal-independent background timing calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 2, pp. 620–633, Feb. 2022.

[7] Y. Konwar *et al.*, "A 12-bit 8-MS/s SAR ADC based on deterministic dithering in 0.18-μm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 243–246, 2022.

[8] X. Tang, Y. Hu, and J. Chen, "Low-power SAR ADC design: Overview and survey of state-of-the-art techniques," *Microelec- tron. J.*, vol. 128, Art. no. 105534, Dec. 2022.

[9] D. Verma, A. Patel, and P. Jain, "Design of 10-bit asynchronous SAR ADC with on-chip comparator offset calibration," *Sensors*, vol. 22, no. 19, Art. no. 7375, Oct. 2022.

[10] X. Tang *et al.*, "A 28 nm CMOS 10-bit 100-MS/s asynchronous SAR ADC without calibration," *Electronics*, vol. 10, no. 24, Art. no. 3091, Dec. 2021.

[11] A. L. Campos *et al.*, "A 10-bit 0.01-to-12-MS/s asynchronous low-power SAR ADC in 65-nm CMOS," *Analog Integr. Circuits Signal Process.*, vol. 106, pp. 321–337, 2021.

[12] E. Swindlehurst *et al.*, "An 8-bit 21-mW 10-GHz time-interleaved SAR ADC with grouped DAC capacitors and two-path bootstrapped switch," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 83–86, Sep. 2019.